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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,163	09/12/2003	Sung-Fei Wang	10230-US-PA	2162

31561 7590 01/31/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,163	WANG, SUNG-FEI	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *9-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 18-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/605163 Attorney's Docket #: 10230-US-PA
Filing Date: 9/13/2003; claimed foreign priority to 2/26/2003

Applicant: Wang

Examiner: Alexander Williams

Applicant's Amendment filed 11/29/04 to the election with traverse of Species I (claims 1-8 and 18-25) filed 7/2/04 is acknowledged. Applicant's has added claim 26 to this species also.

This application contains claims 9-17 drawn to an invention non-elected with traverse. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01).

Note: In the last office action, the section of the title was not descriptive was in error. The title was in its best form as first presented.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Note: Applicant's arguments in regards to the drawings not showing the heat spreader is plated with gold filed 11/29/04 has been considered but are not found to be persuasive. The art clearly show devices having a semiconductor chip and heat spreaders being plated with gold shown. See cited references.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the wherein the heat spreader is plated with gold in claims 4 and 25 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 4, 24 and 25 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 4 and 25, it is unclear and confusing to what is meant and what shows "wherein the heat spreader is plated with gold." Where is this shown in the drawing? Note: Applicant's arguments in regards to the drawings not showing the heat spreader is plated with gold filed 11/29/04 has been considered but are not found to be persuasive. The art clearly show devices having a semiconductor chip and heat spreaders being plated with gold shown. See cited references.

In claim 24, it is unclear and confusing what is meant and how the heat spreader is without signal transmission functions disposed on the active surface of the first chip and comprising silicon. Is this a metal heat spreader or a silicon heat spreader with signal transmission function basically operating as a dummy chip?

Any of claims 4, 24 and 25 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4 to 8, 18 to 23, 25 and 26, **insofar as claims 4 and 25 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Degani et al. (U.S. Patent # 5,646,828) in view of Nakatani et al. (Japan Patent # 57-32676).

1. Degani et al. (figures 1 to 10) specifically figure 8 show a multi-chip module (MCM) **17**,comprising: a substrate **71** having an opening **72** therein; a plurality of first bumps **(74 connecting 18 to 71)**; a first chip **20** that has an active surface bonded to and electrically connected with the substrate through the first bumps, the active surface of the first chip facing the opening of the substrate; a plurality of second bumps **(74 connecting 20 to 18)**; at least one second chip **20** disposed in the opening of the substrate and bonded to the active surface of the first chip through the second bumps, the second chip being electrically connected to the first chip through the second bumps; and at least one heat spreader **19,73** disposed in the opening of the substrate and bonded to the active surface of the first chip. Degani et al. show the features of the claimed invention as detailed above, but fail to explicitly show the heat spreader comprises a chip without signal transmission functions, wherein the heat spreader is plated with gold.

Nakatani et al. show a high power GaAs field effect transistor. Specifically, Nakatani et al. (figures1a to 2b) specifically figure 2(b) discloses a substrate **6** having an

opening **(portion between the two 6's)** therein; a plurality of first bumps **33**; a first chip **1** that has an active surface bonded to and electrically connected with the substrate through the first bumps, the active surface of the first chip facing the opening of the substrate; a plurality of second bumps **47,22,37**; and at least one heat spreader **5,55** without signal transmission functions disposed in the opening of the substrate and bonded to the active surface of the first chip for the purpose of obtaining a high power by a GaAs FET in high frequencies and removing heat from the FET.

2. The MCM package of claim 1, the combination with Degani et al. further comprising a filling material **29** in the opening of the substrate, between the first chip **18** and the second chip **20** and between the first chip **18** and the substrate **71**, the filling material encapsulating the first bumps **74** and the second bumps **74**.

4 and 25. The MCM package of claim 1 or 18, the combination with Nakatani et al. showing wherein the heat spreader **5,55** is plated with gold (see Nakatani et al.'s constitution).

5. The MCM package of claim 1, the combination with Nakatani et al. further comprising a plurality of third bumps **47,22,37** for bonding the heat spreader **5,55** to the active surface of the first chip **1**.

6. The MCM package of claim 1, the combination with Nakatani et al. further comprising a thermally conductive adhesive **22** for bonding the heat spreader **5,55** to the active surface of the first chip **1**.

7. The MCM package of claim 1, the combination with Degani et al. show wherein the first chip **1** further comprises a ground contact **(inherit)** and the second bumps **(74 connecting 20 to 18)** comprises a ground bump.

8. The MCM package of claim 7, the combination with Nakatani et al. show wherein the heat spreader **5,55** is electrically connected to the ground contact **(inherit)** through the ground bump **(inherit)**.

18. Degani et al. (figures 1 to 10) specifically figure 8 show a multi-chip **17** structure having a chip loaded with at least one other chip and at least one heat spreader, comprising: a first chip **18** having an active surface; at least one second chip **20** disposed on the active surface of the first chip; and at least one heat spreader **19,73** disposed on the active surface of the first chip. Degani et al. show the features of the claimed invention as detailed above, but fail to explicitly show the heat spreader comprises a chip without signal transmission functions, wherein the heat spreader is plated with gold.

Nakatani et al. show a high power GaAs field effect transistor. Specifically, Nakatani et al. (figures1a to 2b) specifically figure 2(b) discloses a substrate **6** having an opening **(portion between the two 6's)** therein; a plurality of first bumps **33**; a first chip **1** that has an active surface bonded to and electrically connected with the substrate through the first bumps, the active surface of the first chip facing the opening of the substrate; a plurality of second bumps **47,22,37**; and at least one heat spreader **5,55** without signal transmission functions disposed in the opening of the substrate and bonded to the active surface of the first chip for the purpose of obtaining a high power by a GaAs FET in high frequencies and removing heat from the FET.

19. The multi-chip structure of claim 18, Degani et al. further comprising a plurality of bumps **(74 connecting 18 to 71)** for bonding the second chip **20** to the active surface of the first chip **18**.

20. The multi-chip structure of claim 19, Degani et al. further comprising a filling material **29** between the first chip **18** and the second chip **20** encapsulating the bumps **(74 connecting 18 to 71)**.

21. The multi-chip structure of claim 18, Nakatani et al. further comprising a plurality of bumps **47,22,37** for bonding the heat spreader **5,55** to the active surface of the first chip **1**.

22. The multi-chip structure of claim 21, Degani et al. further comprising a filling material between the first chip and the heat spreader encapsulating the bumps.

23. The multi-chip structure of claim 18, Nakatani et al. further comprising a thermally conductive adhesive **47,22,37** for bonding the heat spreader **5,55** to the active surface of the first chip **1**.

26. Degani et al. (figures 1 to 10) specifically figure 8 show a multi-chip module (MCM) **17** package, comprising: a substrate **71** having a hole **72** therein; a plurality of first bumps **(74 connecting 18 to 71)**; a first chip **20** that has an active surface bonded to and electrically connected with the substrate **71** through the first bumps, the active surface of the first chip facing the hole of the substrate; a plurality of second bumps **(74 connecting 20 to 18)**; at least one second chip **20** disposed in the hole of the substrate and bonded to the active surface of the first chip through the second bumps, the second chip being electrically connected to the first chip through the second bumps; and at least one heat spreader **19** disposed in the hole of the substrate and bonded to the active surface of the first chip. Degani et al. show the features of the claimed invention

as detailed above, but fail to explicitly show the heat spreader comprises a chip without signal transmission functions, wherein the heat spreader is plated with gold.

Nakatani et al. show a high power GaAs field effect transistor. Specifically, Nakatani et al. (figures1a to 2b) specifically figure 2(b) discloses a substrate **6** having an opening **(portion between the two 6's)** therein; a plurality of first bumps **33**; a first chip **1** that has an active surface bonded to and electrically connected with the substrate through the first bumps, the active surface of the first chip facing the opening of the substrate; a plurality of second bumps **47,22,37**; and at least one heat spreader **5,55** without signal transmission functions disposed in the opening of the substrate and bonded to the active surface of the first chip for the purpose of obtaining a high power by a GaAs FET in high frequencies and removing heat from the FET.

19. The multi-chip structure of claim 18, Degani et al. further comprising a plurality of bumps **(74 connecting 18 to 71)** for bonding the second chip **20** to the active surface of the first chip **18**.

20. The multi-chip structure of claim 19, Degani et al. further comprising a filling material **29** between the first chip **18** and the second chip **20** encapsulating the bumps **(74 connecting 18 to 71)**.

Therefore, it would have been obvious to one of ordinary skill in the art to use Nakatani et al.'s gold plated heat sink chip comprises a chip without signal transmission functions for the purpose of obtaining a high power by a GaAs FET in high frequencies and removing heat from the FET.

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Degani et al. (U.S. Patent # 5,646,828) in view of Nakatani et al. (Japan Patent # 57-32676) and further in view of Osedo (Japan Patent # 3-187227A).

Degani et al./Nakatani et al. combination show the features of the claimed invention as detailed above, but fail to explicitly show the heat spreader comprises a chip without signal transmission functions, wherein the heat spreader comprises silicon.

Osedo is cited for showing a semiconductor device. Specifically, Osedo (figures 1 to 3) disclosing Au plating, solder or conductive adhesive 6 is applied to the bonding surfaces of the metal chips 5 which are bonded to the electrode 3 of the semiconductor chip 1 and the metal chip 5 is bonded to the electrode 3 of the semiconductor chip 1 with it and further, as Au plating, solder or conductive adhesive 6 is applied to the bonded metal chip 5, the metal chip

5 can be bonded to the metal wiring of a package for the purpose of having highly accurate bonding between a semiconductor device and a package side.

3. The MCM package of claim 1, the combination with Osedo showing wherein the heat spreader comprises a chip **5** without signal transmission functions.

Therefore, it would have been obvious to one of ordinary skill in the art to use Osedo's gold plated heat sink chip for the purpose of having highly accurate bonding between a semicondcutor device and a package side.

Response

Applicant's arguments filed 11/29/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claim 1, 18 and 26" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/777,786,734,737,738,723,686,685,678,673,680,774, 784	8/25/04
Other Documentation: foreign patents and literature in 257/777,786,734,737,738,723,686,685,678,673,680,774, 784	8/25/04
Electronic data base(s): U.S. Patents EAST	8/25/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
1/28/05

Primary Patent Examiner
Alexander O. Williams